Lateral dopant profiling with 200 nm resolution by scanning capacitance microscopy

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Measurement of dopant density in silicon with lateral resolution on the 200 nm scale has been demonstrated with a near-field capacitance technique. The technique is based upon the measurement of local capacitance between a 100 nm tip and a semiconducting surface. Lateral dopant imaging is achieved by the measurement of the voltage-dependent capacitance between tip and sample due to the depletion of carriers in the semiconductor, as the tip is scanned laterally over the surface. Measurements of dopant density have been demonstrated over a dopant range of 10^{15}–10^{20} cm^{-3}. Capacitance-voltage measurements have been made on a submicrometer scale.

Accurate knowledge of impurity dopant profiles in three dimensions (3D) is necessary for the design and characterization of both metal-oxide semiconductor field-effect transistor (MOSFET) and bipolar devices in state-of-the-art silicon technology. At the current level of integration, MOSFET device dimensions can occupy an area of less than $10\,\mu m^2$. In the active region of a MOSFET device, the impurity dopant profile in the junction region between the source/drain and the gate (Fig. 1) is tailored over a concentration range, typically of 10^{15}–10^{20} cm^{-3}. This gradient can occur over a spatial extent of 500 nm or less in both the vertical and lateral directions. Characterizing this dopant profile is a major challenge for device designers.

Unfortunately, there has been no method which is capable of measuring 3D profiles quantitatively in a straightforward, reliable, and repeatable (nondestructive) way. To date, the methods which have been developed, such as junction-staining[1] or transmission electron microscopy,[2] generally yield only qualitative information. Others have been proposed, such as a matrix of secondary-ion mass spectrometry[3] measurements. All these methods are time and labor intensive, and they are destructive to the sample. It is noteworthy that the exception among the standard one-dimensional (1D) methods is the capacitance-voltage (C-V) technique[4] which is both nondestructive and quantitative.

We present here a technique for measuring dopant profiles which is designed to fulfill all of the above criteria. It is, in fact, an extension of the classic C-V technique on a very local scale using near-field principles. It is based upon the detection of the capacitance between a 100 nm tip and a semiconductor surface. When the tip is biased so as to deplete the surface, the measured depletion capacitance provides the necessary information to determine the local activated dopant density. Previous work in the area of scanning capacitance microscopy[5–8] has focused on the measurement of topographical and dielectric properties of metallic and insulating surfaces. Here, we provide the first demonstration of dopant imaging and C-V measurement in semiconductors on a submicrometer scale.

As depicted in Fig. 1, a small metallic probe, with a radius of curvature at its tip of typically 50 nm, is scanned over the nonuniformly doped sample. A bias voltage (dc or ac) is placed on the tip, and the local depletion capacitance C or its derivative ($\partial C/\partial V$) are then measured as a function of lateral position (x). The measured capacitance or capacitive gradient as a function of bias voltage provides a direct measurement of the local activated dopant density with high spatial resolution. The data can be deconvolved in a straightforward fashion to obtain a first approximation to the actual ionized dopant profiles.

The experimental system used to demonstrate lateral dopant profiling is seen in Fig. 2. The heart of the system is a capacitance sensor[5,8] which can measure capacitive changes between tip and sample on the order of 3×10^{-22} $F/\sqrt{Hz}$. In order to perform measurements on a small scale, the tip is controlled by a feedback loop, which maintains the capacitive signal constant as the tip is scanned across the surface. To avoid the large, low-frequency drifts in the capacitance output caused by stray capacitance variations, a vertical dither is placed on the tip/sample spacing at typically 30 kHz, providing the means to measure the signal ($\partial C/\partial z$), where z is the vertical dimension, at a frequency where drift and noise is low. This ac signal is sent to a lock-in amplifier, where it is filtered and rectified. The lock-in output is then sent to a standard integrating feedback loop. The loop acts to maintain the ac capacitance signal constant by changing the vertical height of the tip as it is scanned laterally over the surface. The feedback loop operates with an approximately 500 Hz bandwidth. This system has recently achieved surface profiling with 25 nm resolution.[8] The vertical tip control signal is sent to a scan synchronized image display. A

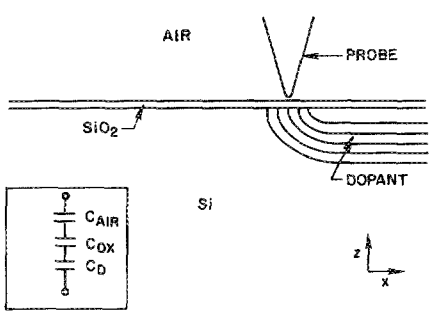

FIG. 1. Illustration of the basic concept of near-field lateral dopant profiling.

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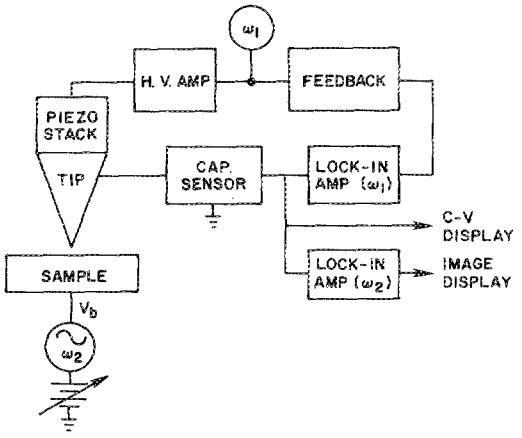

FIG. 2. Experimental arrangement of the capacitance microscope with sample bias voltage.

piezoelectric tube is used to perform the lateral scan. It has a range of 6 mm laterally and 3 mm vertically.

A signal generator provides an ac and/or dc bias voltage between tip and sample at an arbitrary frequency. This voltage makes it possible to obtain a C-V curve at any given position on the sample, or to make $\partial C/\partial V$ images at constant dc bias voltage as the tip is scanned over the surface. A second lock-in amplifier is used to measure the $\partial C/\partial V$ signal, and this information is sent to a second scan synchronized display. The scan and data collection are controlled by a laboratory computer. Both topographic ($\partial C/\partial z$) and $\partial C/\partial V$ images can be simultaneously acquired and displayed on a conventional display monitor. The tips were made by electrochemically etching 0.010 in. tungsten wires in a 2 M NaOH solution. Scanning electron microscope images demonstrate that tip diameters could be as small as 50 nm.

Two samples were used in these experiments. Both were n-type silicon substrates with 24 nm of thermally grown oxide on the surface. The wafers were masked with a thick photoresist grating structure with an 8 μm period, and implanted with BF_2 at 50 keV at a dose of 10^{15} cm^{-2}, producing a peak, p-type dopant density at the surface of 10^{20} cm^{-3}. The photoresist was then stripped from the surface, leaving a topographically flat, nonuniformly implanted silicon surface covered with 24 nm of thermal oxide. The first wafer was thermally annealed at 900 °C for 10 min, whereas the dopant in the second wafer was activated by rapid thermal annealing at 1000 °C for 10 s.

Figure 3 contains the data taken as the tip is scanned across the dopant grating on the first sample. The data displayed are taken from the second lock-in amplifier and represent the magnitude of the $\partial C/\partial V$ signal versus sample position. The three traces are taken at three different dc bias voltages on the sample. The line traces clearly visualize the dopant variation in the sample on a scale below 1 μm. The periodic variation is seen to have an 8 μm repeat distance. The signal varies strongly with the bias voltage, as expected from C-V analysis. The largest signal comes from the lightly doped region, due to the fact that the capacitive variation with bias voltage ($\partial C/\partial V$) is largest at low dopant densities. Note that there is some defect or nonuniformity in the fourth

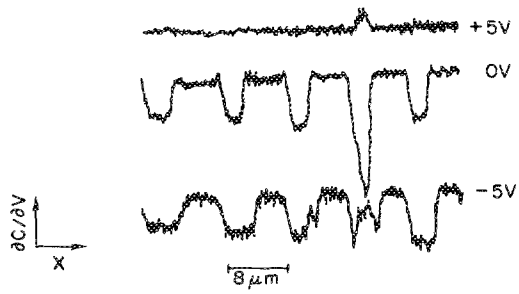

FIG. 3. Three line scans displaying the dc/dv signal at different bias voltages as the tip is moved across the dopant grating.

period of the data, which has apparently shifted the depletion voltage. This could be the result of charge in the oxide.

On the second sample, several sets of C-V curves were taken at various points along the dopant grating. These data are shown in Fig. 4. When the tip is in the center of the low doped region, the C-V curve looks very much like the classical high-frequency C-V curves out of a textbook. As the tip is moved toward the implanted region, however, the C-V curves differ from the ideal 1D curves. A gradual transition in the curves can be seen as the tip moves from the low doped (10^{15} cm^{-3}) n-type region toward the highly doped (10^{20} cm^{-3}) p-type region. These effects are believed to be the result of lateral depletion of the surface. Even though curves B and C are taken at a distance of greater than 0.5 μm from the implant edge, they are modified by the proximity of the high-density dopant region. This is consistent with a simple calculation, which shows that the maximum depletion length in the low-doped region is 0.87 μm. When the probe tip is small compared to this depletion depth, the geometry is more like a spherical than a parallel-plate capacitor, and lateral effects can be significant. When the tip is positioned over the highly doped p-type region and far from the implant edge, the slope of the capacitance versus voltage signal is reversed and much smaller than in the low doping case as predicted by C-V theory.[4] This slope has been measured but cannot be clearly displayed on the scale of Fig. 4.

When a small tip is far from the implant edge, it is expected that even under conditions of spherical depletion, the C-V curves should be similar to those predicted by one-di-

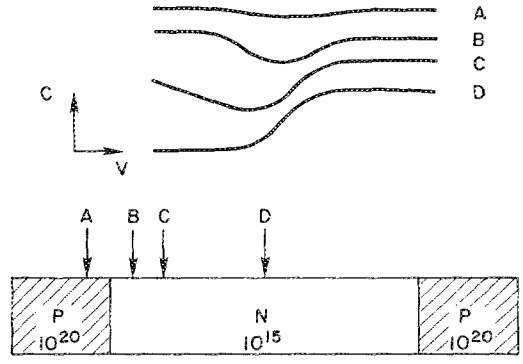

FIG. 4. Series of C-V measurements (-5 to $+5$ V) taken at different points along the dopant grating.

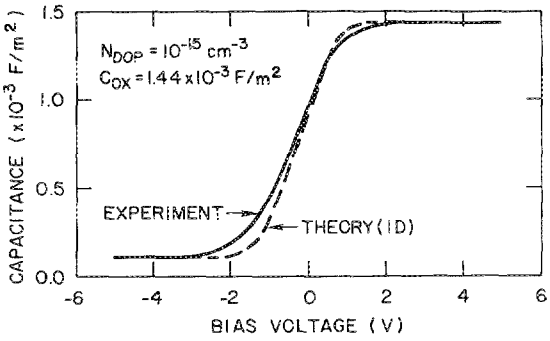

FIG. 5. Experimental C-V curve compared with a 1D calculation of capacitance vs voltage.

mensional calculations. When account is taken for the finite ac measurement voltage (± 0.5 V) used in these experiments, the fit between 1D theory and experiment is reasonably good (see Fig. 5). One fitting parameter was used to account for the tip size.

A third measurement was performed by raster scanning the tip over a region close to the implant, and recording the two-dimensional image of the $\partial C/\partial V$ output at a fixed bias voltage. This result is shown in Fig. 6. The scan area is approximately 3 μm. The transition from low to high doping appears to take place on a 200 nm scale. There are also less apparent variations seen in the low-doped region which are on a similar scale.

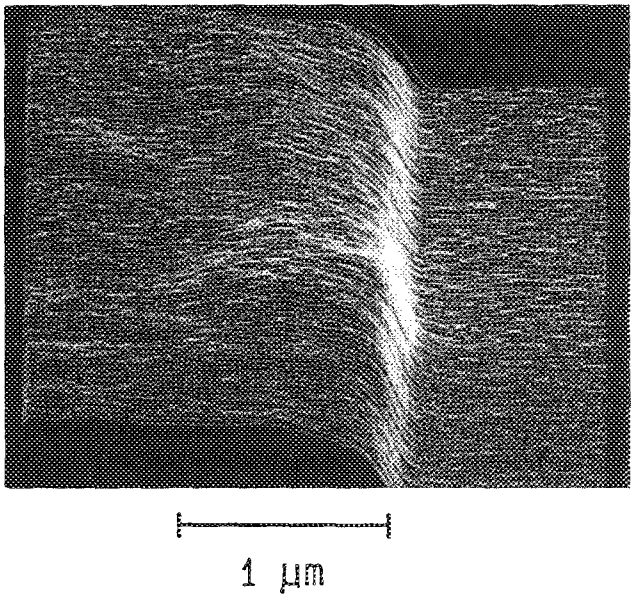

FIG. 6. Image of the edge of the dopant grating. The line scans represent the $\partial C/\partial V$ signal.

Other observations have been made with the capacitance probe. As would be expected, the capacitance signal depends upon the amount of light which is illuminating the silicon. When a 1 mW laser beam (0.633 nm) is focused onto the tip and sample, both the amplitude of the $\partial C/\partial V$ signal and the apparent location of the lateral depletion edge are significantly modified by the light. We believe that these effects are due to the creation of electron-hole pairs, which reduce the depletion effect both in the vertical and lateral dimensions. The measurement of these effects cannot be detailed in this short letter.

In summary, lateral dopant profiling in silicon has been achieved on a 200 nm scale by a nondestructive simple technique. Direct capacitance versus voltage measurements can now be made on a scale which will be useful for device characterization. These measurements extend previous nondestructive measurement capability by more than two orders of magnitude. With further improvements, achievement of dopant imaging on a 10 nm scale is possible. In addition, several other important measurements can be made, including the measurement of trapped charge (for example, in the oxide or at the semiconductor interface), detection of surface defects, direct measurement of a variety of device capacitances, and perhaps even measurement of carrier generation and recombination rates. We feel that this new capability will impact many areas of semiconductor technology.

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